

Additive lithographic fabrication of a Tilt-Gaussian-Vortex mask for focal plane wavefront sensing

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ABSTRACT

Reactive-ion etching (RIE) based lithography has been the prevailing technology for the fabrication of diffractive optical elements (DOEs). However, the inherent physical effects, such as RIE lag and aspect ratio dependent etching, make it challenging to produce spatially-varying features with uniform depths in large areas. In this work, we propose an additive lithographic fabrication process for a reflective Tilt-Gaussian-Vortex (TGV) mask for focal plane wavefront sensing. The unique design of the TGV mask requires simultaneous presence of feature sizes ranging from micrometers to millimeters with low surface roughness. The proposed additive fabrication eliminates the error-prone RIE step after lithography, but instead, a sputter deposition and bi-layer liftoff step is fine-tuned to form the microstructures. Compared to removing materials from the substrate in RIE, our method grows materials up onto the substrate. The combination of sputter deposition and liftoff is uniform across the whole wafer area, resulting in high surface quality and depth accuracy. We demonstrate the effectiveness of the fabrication method by a reflective TGV mask with aluminum deposition on a fused silica substrate. The central Gaussian pattern has a diameter of $130\ \mu\text{m}$ with minimum spacing of $2\ \mu\text{m}$, and the background vortex pattern is $3\ \text{mm} \times 3\ \text{mm}$, with the largest flat region spanning $1.5\ \text{mm}$. A preliminary 4-level prototype has been tested in the Gemini Planet Imaging calibration unit upgrading project, and an improved 16-level sample has been measured. The results show uniform depth and surface roughness control for both the Gaussian and Vortex patterns.

Keywords: Additive lithography, etching-free, sputter, bi-layer liftoff, wavefront sensing

1. INTRODUCTION

Diffractive optical elements (DOEs) are a class of compact optical components with typical feature sizes approaching the operating wavelengths. Owing to their powerful ability to modulate the phase of light, DOEs have been widely adopted in various applications, including optical imaging,^{1,2} holography,³ wavefront sensing,⁴ and so on. Conventionally the continuous profiles of DOEs can be approximated by multi-level binary structures and fabricated by a couple of iterations of the basic photolithography and reactive-ion etching (RIE) steps.^{5,6} For example, by repeating N iterations of the basic fabrication steps, 2^N levels of microstructures can be formed on the substrate. Typically 16-level DOEs (4 iterations) would yield sufficient diffraction efficiency^{7,8} for a host of optical applications.

Despite its dominance in DOE fabrication, RIE based lithographic fabrication suffers from a few inherent drawbacks. First, it is designed to fabricate transmissive DOEs. To produce reflective DOEs, an additional metal coating step would be necessary after the etched structures are finished. Fine but key features may not be well preserved in the final reflective mode. Second, topological accuracy is difficult to achieve when millimeter and micrometer structures are present on the same design. This is because RIE inherently suffers from RIE lag, aspect ratio dependent etching (ARDE), and various etching artifacts, e.g., trenching, faceting, spearheading, rounding, and notching.^{9,10} RIE lag leads to shallower etching depths for smaller structures compared with larger

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features on the same substrate. Etching rate slows down as the etching process carries on, such that the same etching time would result in shallower depths. In addition, the etching artifacts usually take place at the bottom of the etched regions, giving rise to unwanted scattering effects. It is therefore very challenging to fabricate uniform fine features, in particular for mirror-like surface finishes. Third, the microsurface roughness is difficult to maintain for large areas, since the plasma bombardment is more difficult to control for large opening areas on the substrate. Hence, it is challenging to employ conventional etching based lithography for the fabrication of reflective DOEs with spatially-varying features in high surface quality.

In this work, we report an alternative lithographic fabrication method for reflective DOEs by growing metal materials onto the substrate, instead of removing materials from it.¹¹ In other words, we adopt an additive fabrication routine to overcome the limitations and mitigate the artifacts caused by the etching fabrication method. The target material, Aluminum (Al), is directly deposited onto a fused silica substrate by sputtering followed by a bi-layer liftoff.^{12,13} By taking advantage of the binarization, we can fabricate 16-level DOEs with 4 iterations of the liftoff process. We can thoroughly eliminate the etching steps with the proposed additive fabrication method. The benefit of deposition is that the thickness of the deposited metal can be well controlled by the exact deposition time with nanometer accuracy. The uniformity of the deposition process allows for accurate and uniform depth control for both large (millimeter scale) and small (micrometer scale) features at the same time. Low surface roughness is obtained due to the robust deposition, compared with plasma etching. We fabricate a Tilt-Gaussian-Vortex (TGV) phase mask for focal plane wavefront sensing in astronomy applications.^{14–17} The unique design of the TGV mask requires simultaneous presence of feature sizes ranging from micrometers to millimeters with low surface roughness. The central Gaussian pattern has a diameter of 130 μm with minimum spacing of 2 μm , and the background vortex pattern is 3 mm \times 3 mm, with the largest flat region spanning 1.5 mm. The measurement results demonstrate the effectiveness and high quality of the fabrication method. We envision the presented additive lithographic fabrication method would be a practical alternative for reflective DOE fabrication.

2. FABRICATION WORKFLOW

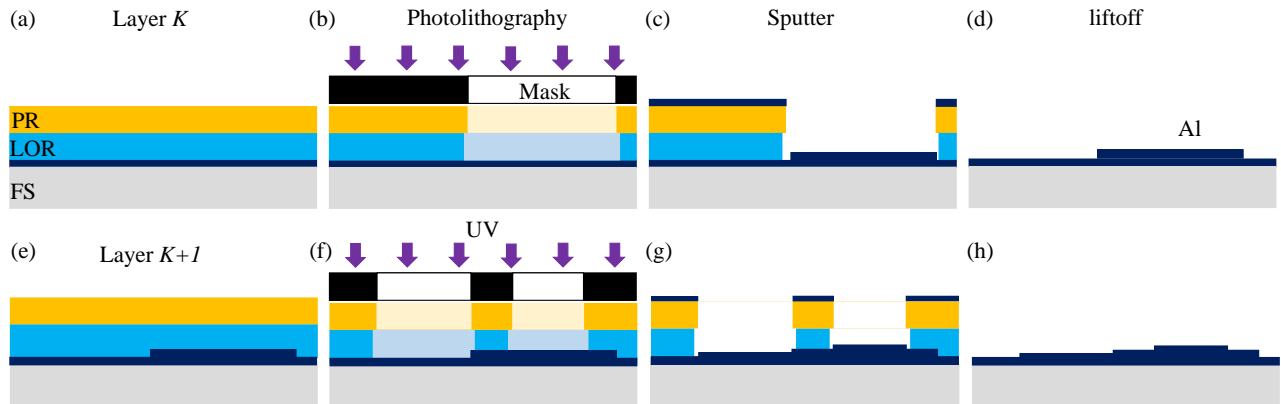


Figure 1. Additive lithographic fabrication workflow. (a) A bi-layer photoresist is spin coated onto the fused silica wafer for Layer K with previously deposited Al structures. (b) The design patterns are transferred from the master mask to the photoresist by UV exposure with photolithography techniques. The exposed areas are removed by developer. (c) Al is selectively deposited into the opening areas by sputtering onto the existing layers. (d) The final patterns are left after the auxiliary photoresist and metal are removed by liftoff. (e)-(f) repeat the process of the deposition-liftoff cycle for Layer K + 1. It can be repeated for N iterations to achieve 2^N -level structures. PR: photoresist. LOR: liftoff resist. Al: Aluminum. FS: fused silica. UV: ultra violet. Redrawn from.¹¹

2.1 Overview

We adopt an additive lithographic fabrication workflow for reflective DOEs.¹¹ Compared with conventional RIE based lithography, we keep the photolithography step for pattern transfer, but employ sputter deposition and bi-layer liftoff subsequently to replace the RIE step. The key steps to form the microstructures is via “additive”

sputter deposition, instead of “subtractive” etching. The basic deposition-liftoff cycle can be repeated N times to fabricate 2^N -level structures. We illustrate two cycles of the fabrication process in Fig. 1. In the beginning of each fabrication cycle, a bi-layer resist, photoresist (PR) above liftoff resist (LOR), is spin coated onto existing structures successively, as shown in Fig. 1(a) for the K-th layer. The photolithography step is the same as in conventional lithography, in which the design patterns are transferred from the master mask to the PR and LOR layers under UV exposure. After development, an undercut profile is created in the bi-layer resist structure, as shown in Fig. 1(b). Aluminum is then sputter deposited onto the existing layers on the substrate, with the unexposed areas protected by PR and LOR, as shown in Fig. 1(c). Finally the auxiliary resist and residual metal are removed by liftoff, leaving the desired patterns on the substrate, shown in Fig. 1(d). The basic deposition-liftoff cycle can be repeated for a couple of times for multi-level structures. For example, Layer K + 1 is shown in Figs. 1(e)-(h). In the following, we first introduce the detailed recipes for each step, and summarize the overall workflow in the end.

2.2 Workflow

The overall workflow is summarized in Table 1. Before the additive fabrication, the fused silica wafer is cleaned in piranha solution for 10 min at 115°C, and then dried in a wafer drier for 7 min. A base layer of Al is deposited by sputtering on the bare wafer for 100 nm. The core fabrication cycle is repeated from Step 4 to Step 15 for the required N times, which will be explained as follows.

Table 1. Additive lithographic fabrication workflow

Step	Work	Tools/Chemicals	Recipe
1	wafer cleaning	Piranha solution	10 min at 115°C
2	wafer drying	wafer drier	7 min
3	base layer deposition	sputter	100 nm
4	wafer dehydration	hotplate	5 min at 200°C
5	adhesion promotion	HMDS vapor prime	20 min at 115°C
6	LOR5B spin coating	spin coater	0.6 μm , 1500 rpm
7	soft bake	hotplate	3 min at 180°C
8	AZ1505 spin coating	spin coater	0.5 μm , 3000 rpm
9	soft bake	hotplate	1 min at 100°C
10	UV exposure	contact aligner (EVG6200)	9 mJ/cm ²
11	development	AZ726MIF	18 sec
12	metal deposition	sputter	time depends on thickness
13	liftoff	DMSO	soak at 80°C
14	sonication	ultra-sonicator	5 - 10 min
15	wafer cleaning and drying	acetone and nitrogen gun	manual cleaning
16	repeat Steps 4 - 15 for multi-level structures		

2.3 Bi-layer photoresist

In conventional photolithography, a single layer photoresist is usually used as the mask to transfer the design patterns onto the substrate in the RIE step. It is sufficient to do so, as the gases in the RIE chamber would not hinder the residual photoresist from being removed afterwards. However, in the proposed method, we create the desired patterns by additive deposition of metals onto the entire resist, and want to remove the residual PR, LOR and metal easily in the liftoff step. For a common positive photoresist, the exposure creates an outward sidewall, or overcut, in the opening areas, as shown in Fig. 2(a). When the metal is deposited, the entire areas are covered by the thin metal film, including the sidewalls. The residual metal on the sidewall may hinder the liftoff chemicals from entering the PR, leading to unsuccessful liftoff. To overcome this problem, we use a combination of LOR, and positive PR, known as the bi-layer structure, to create a re-entrant profile, as shown in Fig. 2(b). Since the development rates for LOR and PR are slightly different (LOR faster than PR), an undercut is available between the two. This structure facilitates the following liftoff step by allowing the liftoff chemicals to flood in more easily.

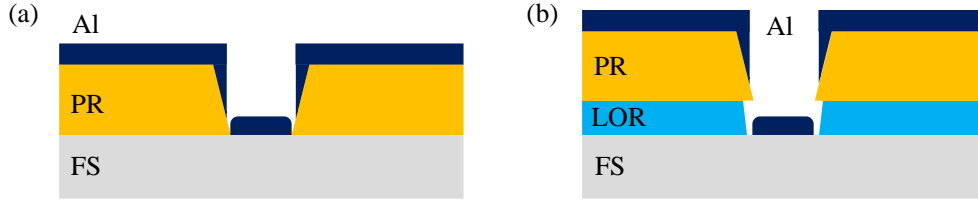


Figure 2. Bi-layer photoresist profile. (a) Conventional positive photoresist has an outward sidewall profile which is covered by the deposited metal. The metal on the sidewall makes it difficult for successful liftoff. (b) A bi-layer resist creates undercut in the resist sidewalls. Sufficient space in the re-entrant profile allows for the liftoff chemicals to completely remove all the resist.

We use a combination of LOR5B (Kayaku) and AZ1505 (MicroChemicals) for the bi-layer resist. The thickness of the LOR5B layer is $0.6 \mu\text{m}$ at 1500 rpm, and the AZ1505 is $0.5 \mu\text{m}$ at 3000 rpm. We optimize the softbake time, temperature and development time to create $1 \mu\text{m}$ undercut, which is necessary for minimum $2 \mu\text{m}$ features. LOR5B is baked at 180°C for 3 min, and AZ1505 is baked at 100°C for 1 min.

2.4 Photolithography

Given a design phase, we first generate a series of N binary patterns by slicing the phase function by a factor of $1/2$ successively. This results in mask patterns in a course-to-fine way. These patterns are used to fabricate N master masks by laser direct writing. We use Heidelberg DWL2000 to make these masks on 5-inch blank soda lime substrates (Nanofilm).

We use 4-inch, 0.5 mm-thick fused silica wafers as the sample substrate. The wafer is first dehydrated on a hotplate at 200°C for 5 min. Before spin coating the photoresist, we apply Hexamethyldisilazane (HMDS) vapor prime to promote adhesion to the substrate. The HMDS step is optional, but we find it helpful to create small features as small as $2 \mu\text{m}$. The HMDS vapor prime is done at 115°C for 20 min. AZ1505 and LOR5B are then spin coated successively with proper softbake.

The design patterns are transferred from the master mask to the photoresist by UV light exposure on a contact aligner. We use EVG 6200 ∞ with i-line UV source in a vacuum+hard mode to project the patterns from the master mask to the photoresist. The exposure dose is fine tuned at $9 \text{ mJ}/\text{cm}^2$ for optimal spatial resolution.

The developer for the resist should be chosen such that the metal structures are not etched during the development step. Since our micro structures are built with Al, the photoresist is developed with AZ726MIF developer. The development time is fine tuned to be 18 sec to fully remove the exposed photoresist, as well as to create sufficient but not excessive undercut for the bi-layer structure.

2.5 Sputter deposition

Aluminum is an excellent yet cost-effective material for reflective coating because of its high reflectance over a wide spectral range. It can also be deposited effectively by sputtering. We use an ion beam assisted sputter (ESCRD4) for Al deposition. The DC power is 400 W, and Argon (Ar) flow is 25 sccm. The process is performed in a vacuum chamber with pressure at 7.5 mTorr. The deposited thickness of Al shows excellent linearity with deposition time, and is nearly independent of feature size, so the thickness can be time-controlled very well to achieve nanometer accuracy. In addition, the deposition thickness is independent of the feature size, resulting in uniform thickness across the whole 4-inch wafer.

2.6 Al liftoff

The auxiliary LOR and PR, and the residual Al on the resist are removed by liftoff. We leave the sample in Dimethyl Sulfoxide (DMSO) soak at 80°C to lift all auxiliary materials off. The liftoff rate for Al is slow, so typically 2 hours are needed for complete removal. It may take overnight for thick Al to be removed. An optional sonication for 5-10 min is helpful to clear residual Al, but care should be taken to prevent metal re-deposition onto the sample surface. Finally the wafer can be cleaned by acetone and dried by N_2 gun manually.

3. TEST RESULTS

We apply the above fabrication workflow to fabricate a reflective DOE designed for focal plane wavefront sensing in astronomy applications. The TGV phase mask consists of a central tilt and Gaussian phase, and a background vortex phase. The unique challenge of the TGV design requires simultaneous presence of feature sizes ranging from micrometers (Tilt-Gaussian) and millimeters (Vortex). The surface roughness should be kept as low as possible (in the nm scale) on both small and large features. Previously a preliminary 4-level prototype has been tested.^{16,17} In this work, we demonstrate an improved 16-level sample with better fabrication quality.

3.1 Tilt-Gaussian-Vortex phase

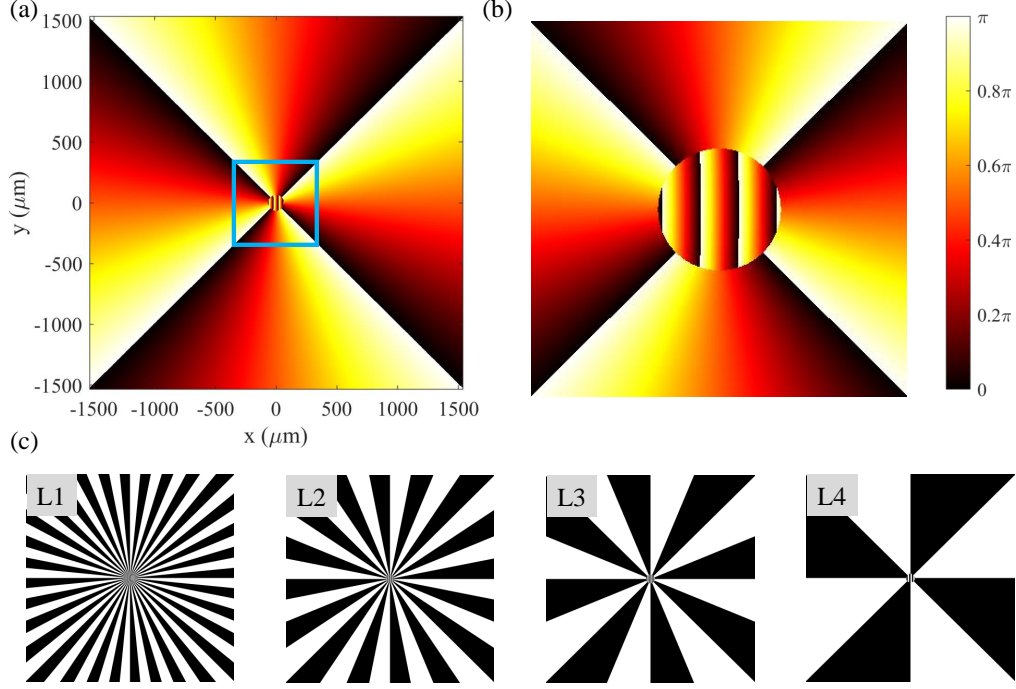


Figure 3. The TGV phase function and binarized masks. (a) The TGV phase consists of a central Tilt-Gaussian phase with fine features and a background Vortex phase with radially expanding features. (b) An enlarged view of the central Tilt-Gaussian pattern. (c) The master masks are generated by slicing the phase function successively by a factor of 1/2. The masks are from fine (L1) to coarse (L4) to make sure the highest resolution can be fabricated well. The accumulated patterns are a close approximation of the continuous design.

The phase function of the TGV design¹⁴ is defined as

$$\phi_{\text{TGV}}(x, y) = T + G + V, \quad (1)$$

where

$$\begin{cases} T = 3.16\xi_0 (x \cos \theta_0 + y \sin \theta_0), & r < e, \\ G = g \exp\left(-\frac{1}{2}\left(\frac{r}{\sigma}\right)^2\right), & r < e, \\ V = l_p \theta, & r > e, \end{cases} \quad (2)$$

where x and y are two-dimensional ramps along x and y in units of λ/D , $r = \sqrt{x^2 + y^2}$, and $\theta = \tan^{-1}(y/x)$. ξ_0 and θ_0 are the tip/tilt parameters. g and σ are the Gaussian amplitude and width parameters. l_p is the topological charge of the Vortex. e is the radius of the Tilt-Gaussian region in units of λ/D . At the wavelength and F-number of the NRC laboratory testing setup, the central Gaussian pattern has a diameter of 130 μm with

minimum spacing of $2\ \mu\text{m}$, and the background vortex pattern is $3\ \text{mm} \times 3\ \text{mm}$, with the largest flat region spanning $1.5\ \text{mm}$. The design wavelength is $1.3\ \mu\text{m}$.

The phase profile is shown in Fig. 3(a). Note that the DOE operates in reflective mode, so the one-way phase in the structure is π , and the effective phase is 2π after reflection. The lateral resolution is $2\ \mu\text{m}$. An enlarged central Tilt-Gaussian pattern is shown in Fig. 3(b). We take a 16-level approximation for the continuous phase, and generate the master masks for each level by slicing the phase function by a successive factor of $1/2$. The four masks are shown in Fig. 3(c), from L1 to L4. L1 has the finest pattern, and L4 has the coarsest pattern. It is clear to see that, the central region requires highest spatial resolution, while the background vortex pattern requires large flat regions. These features should have the same thickness in the final sample, and surface roughness should be kept in the nanometer scale. This is particularly challenging for conventional RIE fabrication, but can be accomplished by the proposed additive fabrication.

3.2 Deposition rate calibration

Before fabricating the 16-level TGV patterns, the deposition rate for Al in the sputter step should be measured. We fix the deposition parameters as shown in Sec. 2.5, and sample the deposition time for 200 s, 400 s, 600 s, and 800 s respectively. The deposited thickness for a test pattern is measured with a Zygo profilometer (NewView 7300). We plot the data in Fig. 4. The result indicates that the deposition thickness is linear with the time period of sputtering. The deposition rate is around $8\ \text{nm}/\text{min}$.

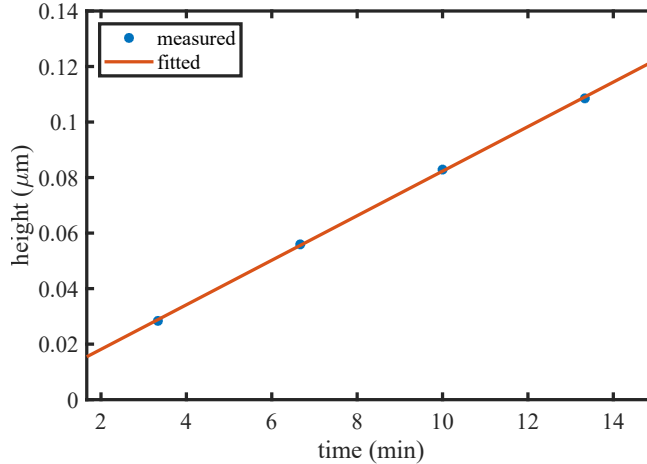


Figure 4. The deposition thickness of Al is linear with time in the test range, resulting in a constant deposition rate.

The total height at the design wavelength is $h_{\text{max}} = \lambda/2 = 650\ \text{nm}$ for the one-way π phase modulation. Each stair of the 16-level approximation is $40.6\ \text{nm}$, so the deposition thicknesses from L1 to L4 are $40.6\ \text{nm}$, $81.3\ \text{nm}$, $162.5\ \text{nm}$, and $325\ \text{nm}$. The height in total is $15h_{\text{max}}/16 = 609\ \text{nm}$. The corresponding deposition periods are 288 s, 593 s, 1185 s, and 2370 s respectively. Note that for longer deposition periods ($> 1000\ \text{s}$), we run the sputtering with separate shorter periods, instead of a single long period. During the intervals, the wafer is pulled out of the chamber to cool down to room temperature before the next period of sputtering.

3.3 Measurements

We characterize the fabricated 16-level TGV sample by the 3D profile measured on a Zygo profilometer (NewView 7300). The results are shown in Fig. 5(a), and with a 5x objective to show the background vortex structures in a larger spatial range in Fig. 5(b). It is observed that the surface quality is reproduced very well for both the central Tilt-Gaussian region and the background Vortex region. It is also consistent from the center to the edges for the whole wafer. Two cross-lines taken from these two regions are plotted in Fig. 5(c) and Fig. 5(d) to compare the real height profile in the center and the edge. The nominal maximum height is $609\ \text{nm}$, and the fabricated heights are $611\ \text{nm}$ in the center and $613\ \text{nm}$ in the edge, respectively. The height accuracy is well within 0.5% across the whole sample. No major artifacts are observed in the fabricated samples.

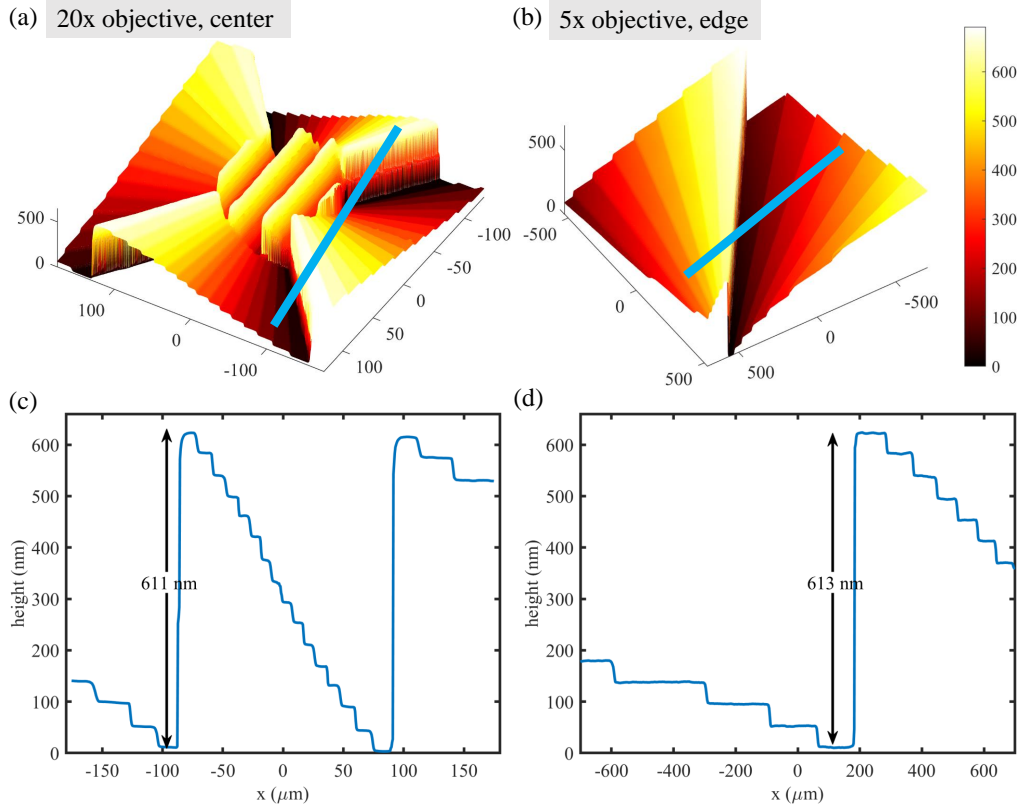


Figure 5. Height profile measurement for the fabricated TGV sample under a Zygo profilometer (NewView 7300). (a) Central Tilt-Gaussian pattern under 20x objective. (b) Background Vortex pattern under 5x objective. (c) A cross-line in (a). (d) A cross-line in (b). The height profiles indicate high accuracy and uniformity of the fabricated sample with respect to the design across the whole sample.

4. DISCUSSION

As seen from the results, the proposed additive lithographic fabrication is able to produce high quality reflective DOEs with simultaneous presence of micrometer to millimeter features in the design. The uniform height profile is challenging for conventional RIE based lithography fabrication, but is guaranteed by our additive deposition fabrication. The optical performance has been verified by a preliminary 4-level TGV sample in our previous work,^{14,16} and the 16-level test is underway.

As a qualitative comparison, we fabricate the same TGV design with conventional RIE based lithography method and the proposed additive fabrication method. The microscopic image of the RIE sample is shown in Fig. 6(a), and the 3D profile is shown in Fig. 6(b). Because of the inherent problems in RIE, the large flat areas in the Vortex region suffer a lot from the low surface roughness, as well as unexpected trenches in some areas. It is also difficult to maintain the fine structures in the central Tilt-Gaussian patterns, even for only 4 levels. On the contrary, our additive fabrication produces high quality surface roughness and keeps good topological structures. The microscopic image of the additive sample is shown in Fig. 6(c), and the 3D profile is shown in Fig. 6(d). A clear improvement is demonstrated from the comparison.

There are also some drawbacks in the current method. We find that around the aligned edges from layer to layer, there may be some residual thin spikes when the deposited thickness becomes large. This effect is feature dependent, not universal across the wafer. The possible reason may be from the liftoff process, in which thin metal film remains on the sidewalls of the PR, but the thickness difference between LOR and Al is not large enough for the DMSO to enter. This could be mitigated with a tall negative photoresist, instead of the bi-layer resist, but may subject to lower spatial resolution. The maximum thickness of the final design pattern is limited

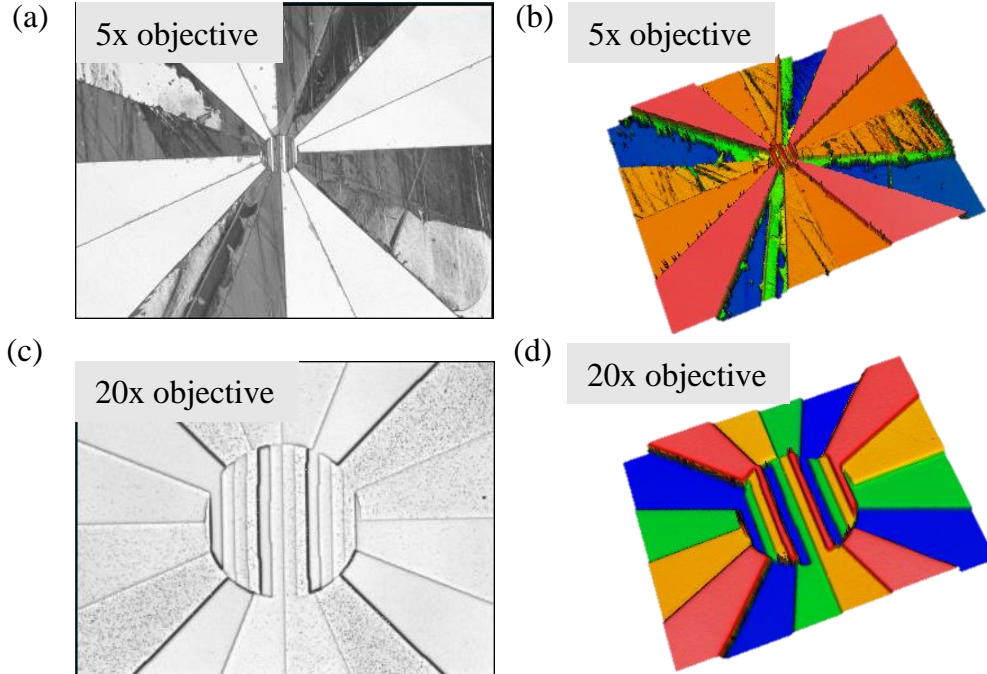


Figure 6. Comparison of fabrication samples for conventional RIE based method and the proposed additive method. (a) Microscopic image of the RIE sample with 5x objective. (b) 3D profile of the RIE sample with 5x objective. (c) Microscopic image of the additive sample with 20x objective. (d) 3D profile of the additive sample with 20x objective.

by the thickness of the LOR5B. It is not possible to achieve a total height that is larger than the LOR thickness. A better combination of PR and LOR is needed for thicker structures.

5. CONCLUSION

Reflective diffractive optical elements with simultaneous fine and coarse features present on the same design is challenging to fabricate with conventional reactive-ion etching method. In this paper, we demonstrate an alternative fabrication workflow with additive lithographic process for this purpose. The proposed fabrication employs sputter deposition and bi-layer liftoff with lithography to realize an etching-free fabrication method. A Tilt-Gaussian-Vortex mask for focal plane wavefront sensing is fabricated by this method. Uniform depth and low surface roughness is achieved and tested. The additive lithographic method could also be used for other types of micro-optics elements with the help of additional pattern transfer steps.

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