Additive fabrication of SiO_2-based micro-optics with lag-free depth and reduced roughness

HADI AMATA,* QIANG FU, AND WOLFGANG HEIDRICH

King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia
*hadi.amata@kaust.edu.sa

Abstract: Ultra-thin optical components with high design flexibility are required for various applications in today's optical and imaging systems, and this is why the use of Diffractive Optical Elements (DOEs) is rapidly increasing. They can be used for multiple optical systems because of their compact size, increased design flexibility, and ease of mass production. Unfortunately, most existing DOEs are fabricated using conventional etching-based methods, resulting in high surface roughness and aspect ratio-dependent etching rate. Furthermore, when small feature size and large feature size patterns co-exist in the same DOE design, the etching depth differs significantly in the same design, called reactive-ion etching (RIE) lag. All these artifacts lead to a reduction in the diffraction efficiency of DOEs. To overcome the drawbacks of etching-based fabrication methods, we propose an alternative method for fabricating DOEs without RIE lag and with improved surface smoothness. The method consists of additively growing multilevel microstructures of SiO_2 material deposited by the plasma-enhanced chemical vapor deposition (PECVD) method onto the substrate followed by liftoff. We demonstrate the effectiveness of the fabrication methods with representative DOEs for imaging and laser beam shaping applications.

1. Introduction

Diffractive Optical Elements (DOEs) have gained significant importance in imaging and display systems over the past few decades. This is mainly because the design and fabrication methods for DOEs have improved to the point that such elements can be encoded to manipulate light in almost any desired direction [1–3]. DOEs consist of amplitude or phase patterns with microstructures, allowing them to perform various functions in various computational imaging systems [4–8].

Nowadays, DOE fabrication utilizes the same fabrication techniques as those in the microelectronics industry. This makes DOE fabrication relatively simple. The main fabrication method combines several photolithography masking and reactive-ion etching (RIE) [1]. Unfortunately, the RIE steps make the fabrication of high-quality DOEs challenging because this technique often hits multiple limitations in achieving consistent and smooth microstructures. These limitations include aspect ratio dependent etching (ARDE), RIE lag, and the presence of various other etching artifacts [9–11]. To fabricate multi-level DOEs, N masks and N process iterations for 2^N levels structure (standard 2^N processing) are needed. Therefore, N etching steps are required, resulting in RIE errors accumulated N time and reducing the DOE diffraction efficiency.

To address these challenges, some researchers developed an approach to build multi-level diffractive structures in photoresists using a single step of additive lithography and multiple digital masking. However, a single-etch step with the required selectivity is needed to transfer the patterns on the substrate [12, 13]. Another additive fabrication method combines metal deposition onto fused silica (FS) substrates by sputtering followed by liftoff to create multi-level reflective DOEs [14]. To achieve transmissive DOEs, the reflective DOEs could serve as a master stamp to transfer the pattern to proper transparent substrates by nanoimprint lithography (NIL) [15]. Although it is feasible to fabricate high-quality reflective DOEs with this additive method, it is still very challenging to build high-quality transmissive DOEs because of the inherent issues of NIL lithography, including the lack of flexibility, poor adhesion of the patterns to the substrate, costs, limited versatility, and poor uniformity throughout large areas [16–18].

In this work, we propose and validate alternative fabrication procedures that eliminate the need for etching and NIL in order to address the aforementioned issues. By the combination of the plasma-enhanced chemical vapor deposition (PECVD) method [19] and bi-layer liftoff lithography [20, 21], we can create DOEs. on Silicon Dioxide (SiO_2) directly. By using standard 2^N processing, we can build multi-level DOEs. Hence, the proposed additive fabrication method needs no etching or nanoimprinting steps. This makes our method a promising candidate to mitigate the challenges related to RIE and NIL processes described above. Also, the PECVD deposited method is known for its excellent deposition rate linearity, which allows a uniform deposition of SiO_2 across the whale wafer, making for both micrometer and millimeter micro-structures. All these advantages make our method an excellent alternative to fabricating transmissive DOEs with high quality.

2. Additive fabrication by SiO_2 deposition and liftoff lithography

In imaging applications, DOEs with computationally optimized phase functions are implemented as height (depth) profiles of microstructures on the substrate, which are then manufactured using photolithography processes. Traditionally, multilevel DOEs are fabricated using the RIE-based method. This method is detailed in our previous work [15]. The technique combines multiple photolithography steps and the same number of etching steps. Unfortunately, this technique accumulates several artifacts [10, 22], including RIE lag, high surface roughness, and other bottom artifacts like spearheading, trenching, and rounding.

In the proposed SiO_2-based additive lithographic method, we eliminate all the subtractive etching steps from the conventional etching-base technique to avoid RIE artifacts. Instead, we replace RIE with an additive PECVD deposition of an optically transparent material (SiO_2) to grow directly the microstructure composing the DOEs on a fused silica substrate.

The proposed method is illustrated in Fig. 1. The fabrication pipeline consists of multiple photolithography steps and multiple deposition and liftoff steps. In the photolithography steps, the glass substrate (FS) is first coated with a stack of Lift Off Resist (LOR) layer and imaging photoresist (PR). Then, we transfer the design patterns on the PR and LOR resist stack by UV exposure. A chemical developer removes the exposed photoresists to create opening areas corresponding to the designed patterns in the two photoresists [20, 21]. After verification under a microscope that the pattern is well transferred on the photoresist, we start the deposition of SiO_2 onto the substrate in the opening areas using the PECVD deposition method. In the last step, the auxiliary LOR and PR layers are removed by N-Methyl-2-pyrrolidone organic solvent (NMP), leaving only the DOE microstructure on the substrate. Figure 1 shows two iterations of the SiO_2-based additive process for a 4-level structure. However, the proposed method could fabricate multi-level DOEs by repeating the basic process for more iterations (e.g., 4 iterations for 16 levels).

3. Results

We present the necessary characterization tests and two example designs to demonstrate the fabrication quality of the proposed additive methods. We study the quality of the thin layer of SiO_2 deposited by the PECVD method and measure the SiO_2 deposition rate before beginning the fabrication workflow. In addition, we show an optical test of a Fresnel lens built with the proposed additive technique and compare it to a similar lens fabricated by the conventional etching method.

3.1. XRD characterization of SiO_2 film

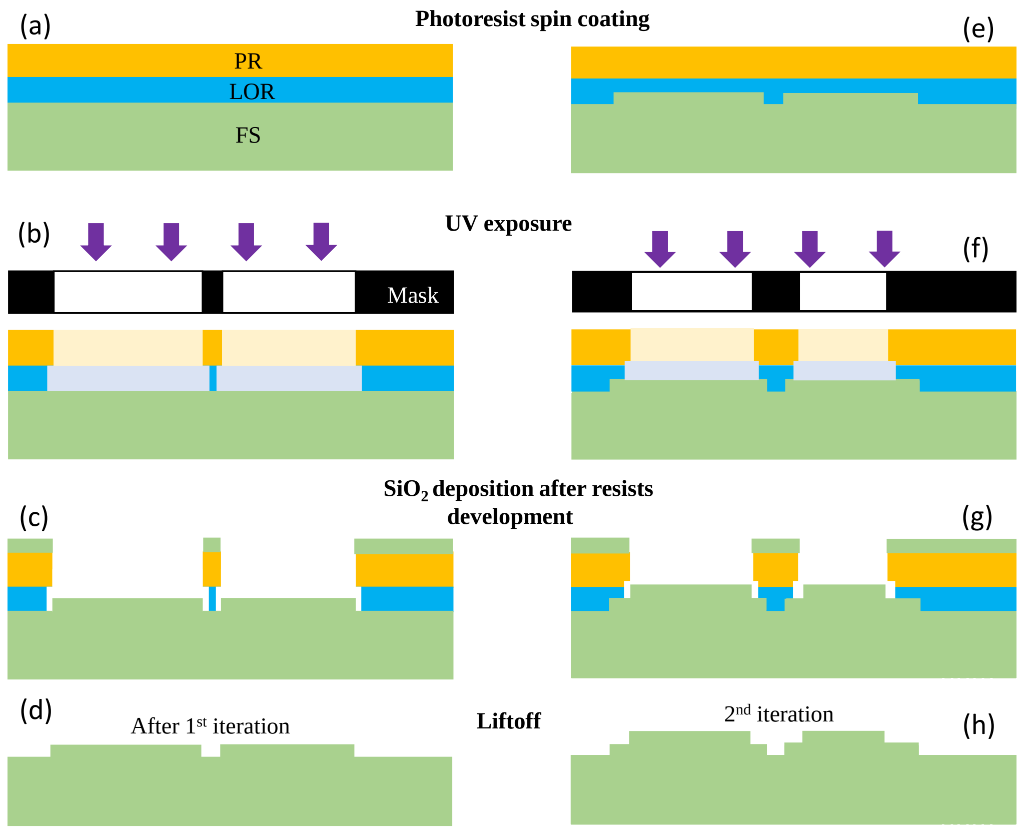

Fig. 1. Standard 2^N processing for multilevel diffractive optical elements fabrication. Each iteration creates 2-level microstructures on the previous profile by applying liftoff lithography followed by SiO_2 deposition. Repeating the fabrication cycle N times can obtain 2^N levels DOE. PR: photoresist. LOR: Liftoff resists. SiO_2: Silicon dioxide. FS: fused silica. UV: ultraviolet.

X-ray crystallography (XRD) characterization has been performed to study the crystallinity of the deposited SiO_2 film by the PECV technique at low temperatures. More precisely, we used the Grazing Incidence Small-Angle X-ray Scattering (GISAXS) technique that employs a grazing incidence geometry, meaning that the incident X-ray beam strikes the sample surface at a very shallow angle (usually less than the critical angle for total external reflection). This shallow angle of incidence maximizes the interaction with the surface, making it sensitive to surface structures and interfaces. Then, GISAXS measures the scattering pattern of X-rays emerging from the sample, and the angle and intensity of the scattered X-rays are analyzed to provide information about the lateral structure, size, shape, and distribution of nanostructures on the surface [23, 24]. Using this technique, we measured the XRD pattern of the deposited 500nm-thick SiO_2 film on the fused silica substrate, shown in Fig. 2.a.

The X-ray diffraction pattern of a 500 nm thick deposited SiO_2 layer shows a broad diffraction peak, indicating that the deposited SiO_2 material is amorphous and composed of nanoparticles of SiO_2 material with sizes ranging from a few nanometers to a few micrometers similar to the bulk SiO_2 and fused [25]. The result is further confirmed by the scanning electron microscopy (SEM) measurement (Fig. 2.b) on the top surface of the tested sample taken by Nova NanoSEM630.

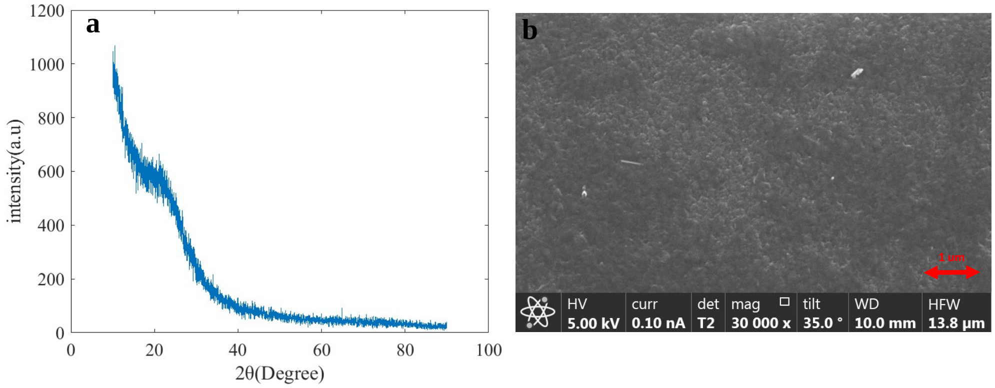

Fig. 2. Characterization of the deposited SiO_2 film. (a) XRD analysis with the Grazing incident X-ray diffraction (GID) technique. (b) The SEM image of the SiO_2 film (top surface).

This makes SiO_2 a good material for the fabrication of micro-optics.

3.2. Deposition rate

SiO_2 deposition is a well-established technique that can be readily implemented using the PECVD [19]. In the test time range, the deposition rate exhibits excellent linearityFig. 3. Therefore, nanometer accuracy of depth is very easy to achieve. Modifying the deposition conditions in the machine process chamber, particularly the RF power and process gas mixture, could increase the deposition rate [19, 19].Additionally, it's important to note that we can establish a fundamental deposition step within a given time and replicate it multiple times if we need to achieve a deposition depth greater than what has been tested.

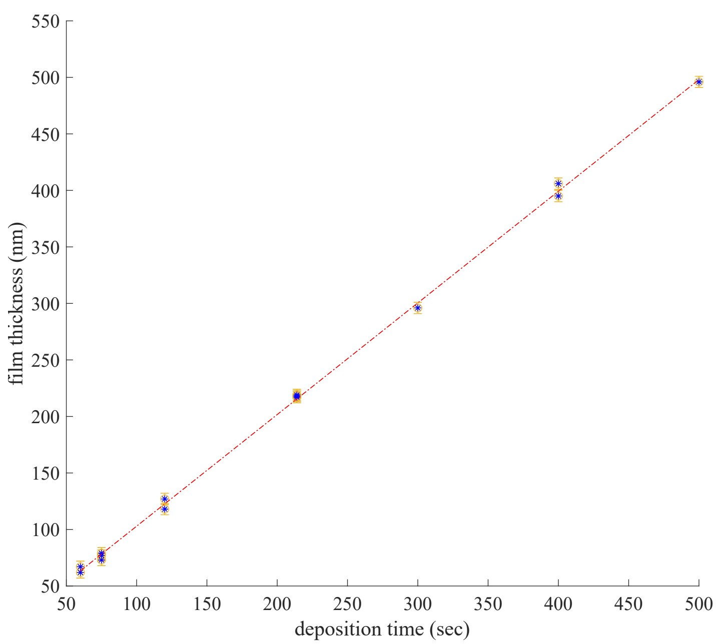

Fig. 3. Deposition rate of SiO_2 by PECVD deposition.

3.3. Surface roughness study

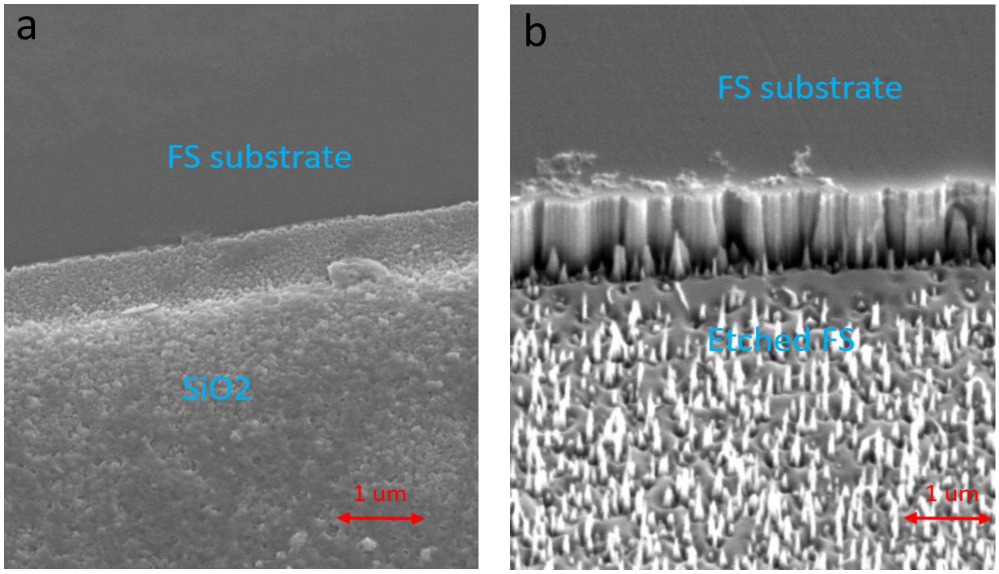

Fig. 4. Surface roughness comparison. (a) SEM image of the deposited SiO_2 by PECVD. (b) The same measurement is done for an etched pattern by RIE.

During the fabrication process of DOEs, multiple fabrication errors inevitably appear, especially with conventional etched base fabrication methods. These errors include RIE lag, aspect ratio-dependent etching rate, and multiple other bottom artifacts [10, 15, 22]. The relationship between manufacturing errors and diffraction efficiency decrease was studied previously [26]. Another simulation study also demonstrated the negative impact of the surface roughness on the efficiency of diffractive optical elements [27]. To compare the surface roughness of the pattern fabricated by the additive and RIE methods, we manufactured two DOEs by both fabrication methods. We used a Nova NanoSEM630 SEM machine and Bruker Dimension Icon Atomic Force Microscope to characterize the two samples. Figure 4 shows an evident improvement in the fabricated pattern surface smoothness. The measured value of the root mean square roughness (RMS roughness or R_q value) is 1.965nm for the SiO_2 film surface and 2.587 nm for the etched fused silica surface. The RMS measure is calculated by taking the average of the measured height deviations taken within the evaluation length and measured from the mean line. This roughness improvement could lead to a significant improvement in DOEs optical performances.

3.4. SiO_2-based DOE Fabrication workflow

The complete workflow of additive DOE fabrication with detailed recipes is shown in Table 1. In the first three steps, the wafer is prepared for the photolithography. There are two steps for wafer decontamination and cleaning using a mixture of sulfuric acid and 30% hydrogen peroxide (Piranha solution) at 115 °C. Then, the wafer is dried for 7 min using a wafer dryer.

To create fine feature sizes in the order of 2 μm, applying an adhesion promotion layer with Hexamethydisilane (HMDS) vapor prime is necessary in Step 3. Then a LOR5B photoresist (Kayaku Advanced Materials, Inc) is spin-coated on the substrate with 1500 rpm speed to gain a thickness of 0.6 μm followed by a soft bake at 180 °C for 3 min in Step 4 and Step 5. In step 6, a 0.5 μm AZ1505 photoresist is spin-coated and soft-baked at 100°C in Step 7.

By using the EVG6200 contact aligner with a dose of 9 mJ/cm^2, the UV exposure is performed

Table 1. SiO_2 additive lithographic workflow

Step	Process	Tools/Chemicals	Recipe
1	wafer cleaning	Piranha solution	10 min at 115°C
2	wafer drying	wafer drier	7 min
3	adhesion promotion	HMDS vapor prime	20 min at 115°C
4	LOR5B spin coating	spin coater	0.6 μm, 1500 rpm
5	soft bake	hotplate	3 min at 180°C
6	AZ1505 spin coating	spin coater	0.5 μm, 3000 rpm
7	soft bake	hotplate	1 min at 100°C
8	UV exposure	contact aligner (EVG6200)	9 mJ/cm^2
9	development	AZ726MIF	18 sec
10	SiO_2 deposition	PECVD	time depends on thickness
11	liftoff	NMP	soak at 80°C
12	sonication	ultra-sonicator	7 - 15 min
13	wafer cleaning and drying	acetone and nitrogen gun	manual cleaning
14	repeat Steps #1 – #13 for multi-level structures		

in Step 8, in hard+vacuum mode. In Step 9, we used an AZ7226MIF developer to develop the LOR-PR bi-layer photoresists. The opening areas are now formed, and the wafer is ready for PECVD deposition in Step 10. The PECVD machine used for the deposition is Oxford PlasmaLab system 100.

In Step 11, we used N-Methyl-2-pyrrolidone organic solvent (NMP) soak at 80°C to remove the residual SiO_2 and auxiliary resists. The lift-off period should be at least 4 hours to ensure complete lift-off. An additional 7-15 min sonication in Step 12 is recommended to ensure residual SiO_2 removal. Finally, the wafer is cleaned and dried with acetone and Nitrogen (N_2) to perform initial microscope quality verification.

We can repeat the fabrication process steps N times to achieve 2^N-levels structure. In our case, the machines we use are limited by a resolution of 1 μm, making it difficult to perform alignment between different layers beyond this limit. In practice, we perform our process $N = 4$ times (16 levels).

3.5. Fabrication examples

Spiral Phase Plate (SPP) In the past decade, optical vortices, or so-called "twisted light," emerged as an important optical element. Recent works show that vortex lenses could be used in many areas, including optical imaging, astronomical observation, optical pattern recognition, and many other areas [28–30]. Spiral phase plate SPP is important in designing optical imaging systems using optical vortices. It is also a very challenging DOE to fabricate with etching-based methods, because the pattern feature sizes differ significantly from the center to the edges (RIE-lag issues). This is why we selected it as our first fabrication example.

We adopt the standard 2^N processing with $N = 4$ to fabricate a three-sector SPP. The phase

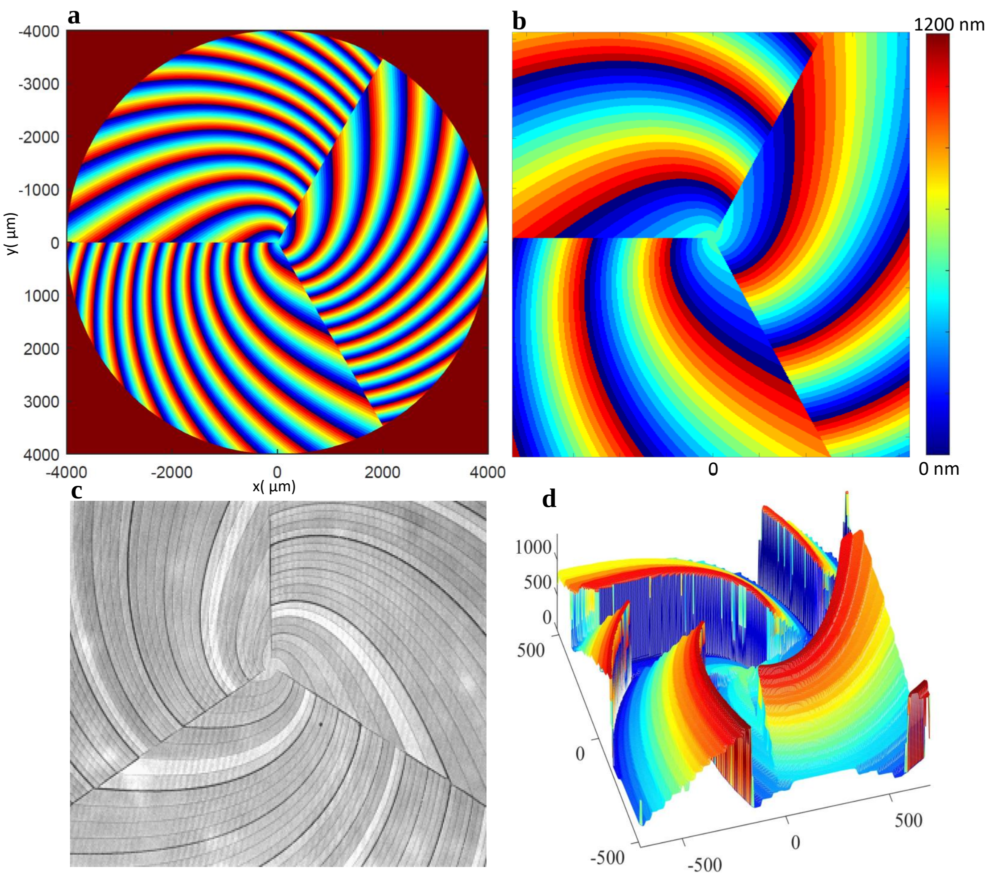

Fig. 5. Spiral phase plate DOE. (a) Continuous designed phase. (b) Discretized 16-level height profile (Zoom in on the center). (c) Microscopic 2D measurement of the fabricated spiral phase (Nikon Eclipse L200N). (d) 3D measurement of the central area of the spiral lens on Zygo profilometer (NewView 7300).

profile is defined in the polar coordinates (ρ, θ) as

$$\phi_{\text{SPP}}(\rho, \theta) = \text{mod}\left[-\frac{2\pi}{\lambda}(n-1)\frac{\rho}{R}H, 2\pi\right], \tag{1}$$

where n is the refractive index, R is the radius of the DOE, and H is a linear ramp along the angular direction,

$$H = H_0 + \frac{3}{2\pi}(H_1 - H_0)\beta, \tag{2}$$

where $\beta = \text{mod}\,[\theta + \pi, 2\pi/3]$ divides the 2D plane into three equal sectors, and

$$\begin{cases} H_0 = 0.5R\tan\theta, \\ H_1 = 2R\tan\theta. \end{cases} \tag{3}$$

Figure 5(a) shows the phase function of the SPP, and Fig. 5(b) represents the discretized 16-level height profile. The deposition heights of SiO_2 are determined by the refractive index of the SiO_2 (n = 1.457) and the operating wavelength. Here, we design the SPP at λ = 550 nm. The maximum height of the deposited SiO_2 is $h_{\max} = \lambda/(n-1) = 1200$ nm for the continuous profile. The radius of the SPP is 4 mm. In the 16-level scenario, the deposited SiO_2 depths on the fused silica wafer are 75 nm, 150 nm, 300 nm, and 600 nm, respectively. We used Zygo NewView 7300 to characterize the fabricated SPP. The results are shown in Fig. 5(c) and (d).

Fresnel lens The second example is the diffractive Fresnel lens, a popular component in many diffractive optics applications [2, 6, 31]. Furthermore, it will give us an easy way to make simple imaging tests without needing other lenses, optical devices, or image post-capture processing. This makes it easier for us to assess the quality of our fabrication method using a simple lens camera configuration [32]. The phase profile of a Fresnel lens is

$$\phi_F(x, y) = \text{mod}\left[-\frac{2\pi}{\lambda} \cdot \frac{(x^2 + y^2)}{2f}, 2\pi\right], \tag{4}$$

where f is the focal length, and λ is the design wavelength. We used the same design parameters as the Spiral Phase Plate, and $f = 100$ mm. Thus, the maximum height of the deposited SiO_2 is 1200 nm, and the radius of the lens is 4 mm.

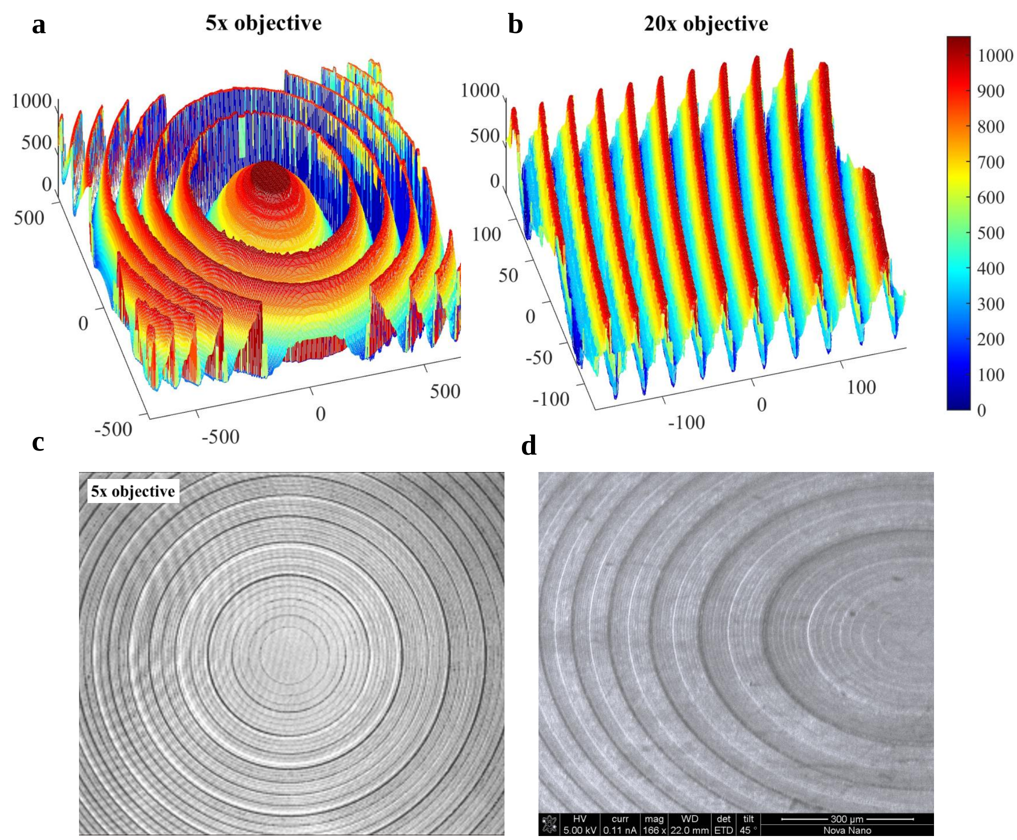

Fig. 6. 3D profile of the fabricated additive Fresnel lens($f = 100mm$). (a) and (b) 3D measurement of the central area and the edge of the fabricated Fresnel lens on Zygo profilometer (NewView 7300). (c) Microscopic 2D measurement of the fabricated Fresnel lens (Nikon Eclipse L200N). (d) The SEM picture of the fabricated Fresnel lens (Nova NanoSEM630).

In Fig. 6 (a)and(b), we show the 3D profile of the fabricated 16-level Fresnel lens in the center and the edges of the lens. It is clear from the results that the fine structures in the center of the Fresnel are well maintained with the same center structure height. This observation is confirmed by a detailed study in Section 3.6 below. Figure 6 (c)and(d) show respectively the Microscopic 2D measurement and the SEM picture of the fabricated Fresnel lens.

3.6. Elimination of RIE-lag artifact through additive fabrication

We fabricated two Fresnel lenses, the first with the conventional RIE method and the second with the proposed additive method. Then, we used the scanning mode of the Bruker Dimension Icon Atomic Force Microscope System to study the depth uniformity across the two DOEs. The obtained results are summarized in the graphs presented in Fig. 7. The results show a difference of around 40 nm between the edge and the center for the RIE lens. In contrast, there is no appreciable change in the depth of the additively fabricated lens. This is a good confirmation that the proposed additive fabrication is an excellent solution for overcoming the RIE-lag issue in the conventional RIE-based fabrication method.

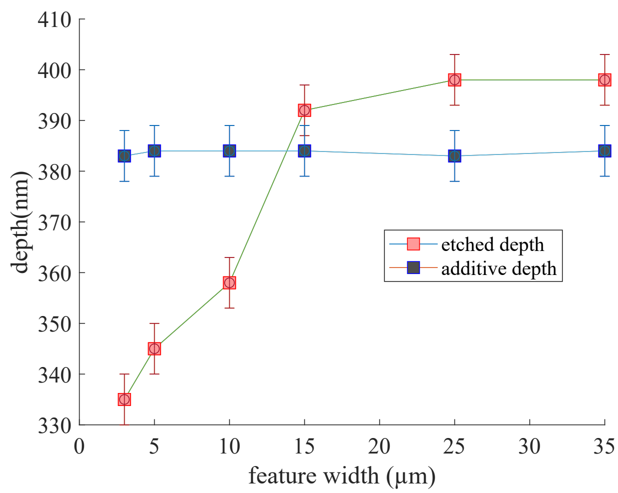

Fig. 7. Etch depth as a function of pattern feature width.

3.7. Imaging test results

Artifacts in the fabrication of DOEs have a direct impact on the diffraction efficiency of these micro-optics, reducing their imaging performance. Fig. 8 shows simple imaging tests we have performed to compare a simple Fresnel lens fabricated by the proposed method with another fabricated by the conventional etching-based method. The results show a reduced haze effect for the additive lens compared to the lens fabrication by the traditional RIE method. This confirms that the improved DOE geometry demonstrated in Sections 3.3 and 3.6 directly impacts the optical performance of the fabricated DOEs.

We emphasize that the paper demonstrates a Fresnel lens's broadband imaging capabilities across the full visible spectrum. Even a perfectly manufactured DOE will exhibit chromatic aberrations. Nevertheless, it's important to highlight that these chromatic aberrations, along with general image degradation or "haze", are significantly diminished in the image acquired using the additively manufactured DOE. This is demonstrated in Fig. 9. This figure shows clearly that the three RGB channels for the intensity profile of the image taken by the fabricated additive Fresnel lens are closer to each other, in contrast to the ones taken from the RIE lens, especially the red and blue color channels.

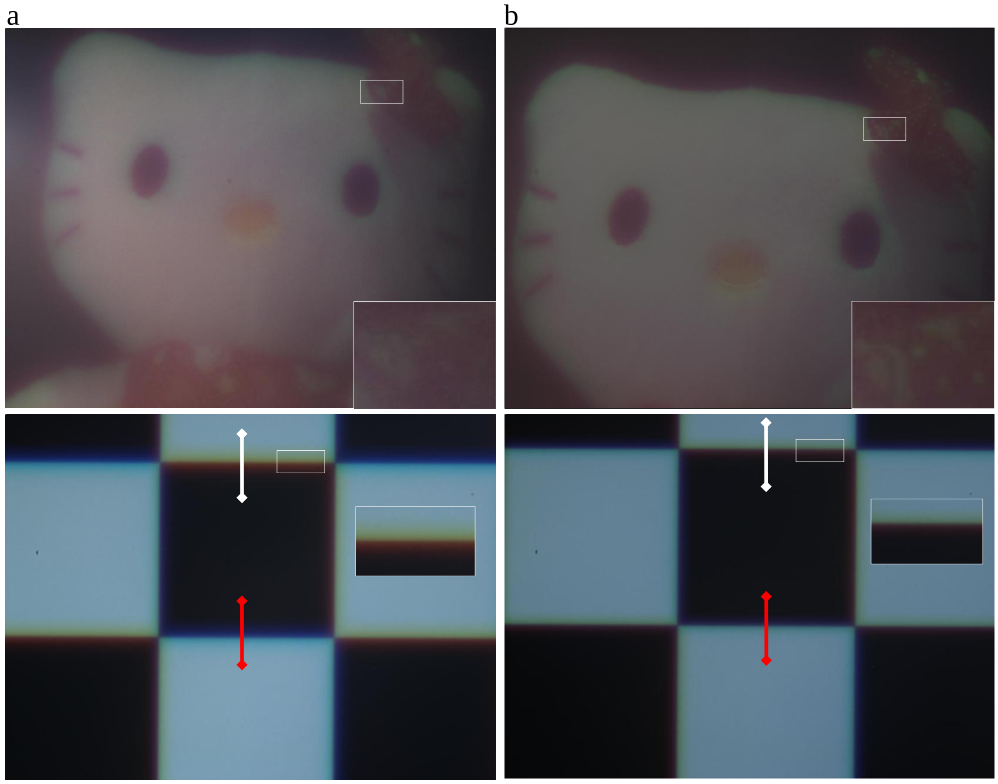

Fig. 8. Imaging test. (a) Image captured with the SiO_2 additive lens. (b) Image captured with the RIE lens.

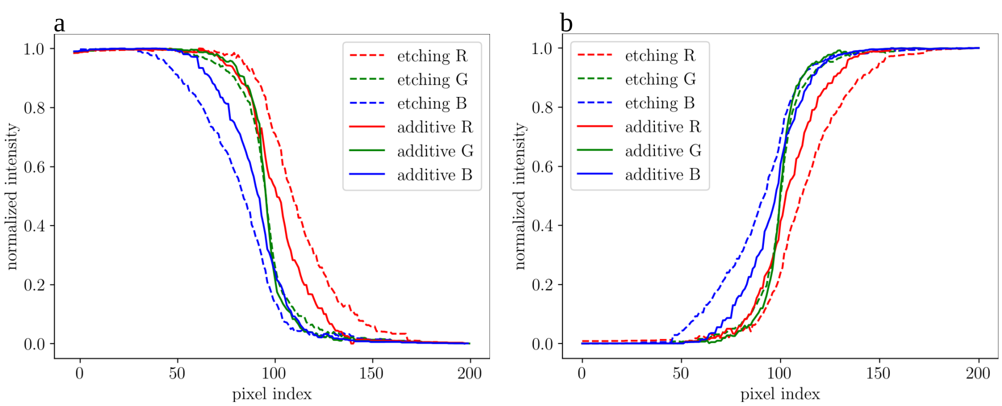

Fig. 9. RGB Intensity profile analysis from the vertical edges between white and black squares of the captured checkerboard image in Fig. 8). (a) From the vertical top edge (white line in Fig 8). (b) From the vertical bottom edge (red line in Fig. 8).

4. Discussion

The results prove that the proposed additive lithographic fabrication method can effectively address various challenging RIE and NIL artifacts. This was confirmed through multiple research studies. First, the roughness study demonstrated a significant improvement in microstructure smoothness with SiO_2 additive lithography. This leads to maintaining the diffraction efficiency of DOEs by reducing the scattering effects. Second, we proved good depth uniformity across a large wafer area with the proposed method, which allows micrometer- and nanometer-scale features to co-exist easily in the same pattern in contrast to the RIE method. The SiO_2 film study shows that the PECVD deposition method gives good optical-quality material and a very stable and linear deposition rate. We also fabricate a single-lens camera prototype using an additive Fresnel lens to test it in actual application. The obtained imaging test results clearly demonstrate the positive potential of the SiO_2-based additive method, with reduced haze in the captured images.

There are several avenues for further improvements of our method. The PECVD deposition of SiO_2 is carried out at a low temperature of 140 °C to maintain the critical dimensions (CDs) of the DOEs pattern because the transition temperature of the liftoff process resists is 200 °C. This limitation directly impacts the quality of SiO_2 film by increasing the film's roughness due to the increased size of the SiO_2 nanoparticles that form the film, compared to fused silica glass, which reduces the optical quality of the SiO_2 film. One potential mitigation would be using thermo-stable photo resists like SX ARP 3500/8 photoresist (Allresist GmbH, Inc.) as the top layer of the bi-layer lift-off. This photoresist is thermally stable up to 300 °C. Second, PECVD material deposition produces nanometer spikes along the side edges of the patterns, especially as the deposited target height increases. This artifact is similar to the liftoff ears reported in the metal deposition by the sputtering method [33, 34]. A possible cause is that the lift-off process may have left a thin SiO_2 deposit on the sidewalls of the PR because the thickness difference between LOR and SiO_2 is insufficient for the developer to pass through. The spikes are very thin and fragile and only emerge when the pattern's feature sizes are a few micrometers in size. Using a mechanical way by pressing DOE into a sheet of soft material, we removed them from a single-level DOE in a recent experiment. This needed to be confirmed for multilevel DOEs in our future work. This operation needs to be repeated N time for N-level DOE. We also explore a chemical way by briefly immersing the sample in Hydrofluoric Acid. The surface roughness of SiO_2 pattern could be improved in the future by adjusting the PECVD parameter as source power, pressure, and bias voltage, as is proven in some work [35].

The proposed technique is developed for visible light imaging applications. However, the technique could be extended to the infrared spectral band by depositing the Silicon material on the Silicon wafer using the same deposition technique (PECVD). Because the maximal material deposition increases with the wavelength $h_{\max} = \lambda/(n-1)$, replacing the resists we used in this work with a thicker liftoff resist is necessary.

Our method is a good alternative for optical device fabrication for research groups using conventional cleanroom instruments. It could also be deployed in the industry because all the process steps are similar to semiconductor device fabrication.

5. Conclusion

A novel additive lithographic fabrication technique for micro-optics has been successfully demonstrated through experimental validation. This method involves the direct growth of an optically transparent material on a substrate that is also transparent. The optical properties of the material are identical to those of the substrate. In contrast to traditional fabrication techniques, the proposed method eliminates the need for substrate material removal through etching or engraving processes. Additive fabrication is a method that does not require a nanoimprint step and the resulting patterns on the substrate serve as the final optical components. The positive results of additive fabrication could overcome the inherent limitations and imperfections often arising from conventional fabrication techniques. This method effectively produced a 16-level spiral phase plate, a diffractive Fresnel lens, and could easily used to fabricate any other DOEs. The results demonstrate that this fabrication method exhibits low surface roughness and better depth uniformity over large pattern areas than the etch-based approach. These improvements are directly visible in the imaging tests of simple Fresnel lenses by significantly enhancing the captured image quality.

Funding. King Abdullah University of Science and Technology (Individual Baseline Funding). KAUST Visual Computing Center operational funding.

Acknowledgments. The fabrication was done in the Nanofabrication Corlabs at KAUST.

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. D. C. O'Shea, T. J. Suleski, A. D. Kathman, and D. W. Prather, *Diffractive optics: design, fabrication, and test* (SPIE Press Bellingham, 2004), vol. 62, pp. 133–148.
2. F. Heide, Q. Fu, Y. Peng, and W. Heidrich, "Encoded diffractive optics for full-spectrum computational imaging," Sci. Rep. **6**, 33543:1–10 (2016).
3. M. Golub, L. Doskolovich, N. Kazanskiy, S. Kharitonov, and V. Soifer, "Computer generated diffractive multi-focal lens," J. Mod. Opt. **39**, 1245–1251 (1992).
4. Y. Peng, Q. Fu, H. Amata, S. Su, F. Heide, and W. Heidrich, "Computational imaging using lightweight diffractive-refractive optics," Opt. Express. **23**, 31393–31407 (2015).
5. M. P. Cagigal and P. J. Valle, "Wavefront sensing using diffractive elements," Opt. Lett. **37**, 3813–3815 (2012).
6. Y. Peng, Q. Fu, F. Heide, and W. Heidrich, "The diffractive achromat full spectrum computational imaging with diffractive optics," ACM Trans. Graph. **35**, 31:1–11 (2016).
7. Q. Fu, D.-M. Yan, and W. Heidrich, "Diffractive lensless imaging with optimized Voronoi-Fresnel phase," Opt. Express **30**, 45807–45823 (2022).
8. Z. Shi, Y. Bahat, S.-H. Baek, Q. Fu, H. Amata, X. Li, P. Chakravarthula, W. Heidrich, and F. Heide, "Seeing through obstructions with diffractive cloaking," ACM Trans. Graph. **41** (2022).
9. S. Lai, D. Johnson, and R. Westerman, "Aspect ratio dependent etching lag reduction in deep silicon etch processes," J VAC SCI TECHNOL A **24**, 1283–1288 (2006).
10. F. Laermer, S. Franssila, L. Sainiemi, and K. Kolari, "Deep reactive ion etching," in *Handbook of silicon based MEMS materials and technologies,* (Elsevier, 2020), pp. 417–446.
11. A. Hadi, F. Qiang, and H. Wolfgang, "Additive diffractive optical elements fabrication by pecvp deposition of sio2 and lift-off process," in *Digital Optical Technologies,* vol. 12624A (Proc. SPIE, 2023).
12. M. Pitchumani, H. Hockel, J. Brown, W. S. Mohammed, and E. G. Johnson, "Additive lithography for refractive micro-optics," in *Micromachining Technology for Micro-Optics and Nano-Optics,* vol. 4984 (Proc. SPIE, 2003), pp. 1–9.
13. M. Pitchumani, H. Hockel, W. Mohammed, and E. G. Johnson, "Additive lithography for fabrication of diffractive optics," Appl. Opt. **41**, 6176–6181 (2002).
14. Q. Fu, H. Amata, B. Gerard, , M. Christian, and W. Heidrich, "Additive lithographic fabrication of a Tilt-Gaussian-Vortex mask for focal plane wavefront sensing," in *OptiFAB 2021,* vol. 11889 (International Society for Optics and Photonics, 2021), pp. 1188911:1–9.
15. Q. Fu, H. Amata, and W. Heidrich, "Etch-free additive lithographic fabrication methods for reflective and transmissive micro-optics," Opt. Express **29**, 36886–36899 (2021).
16. D. Qin, Y. Xia, and G. M. Whitesides, "Soft lithography for micro-and nanoscale patterning," Nat. Protoc **5**, 491–502 (2010).
17. N. S. R. Dongxu Wu and X. Luo, "Nanoimprint lithography - the past, the present and the future," Curr. Nanosci. **12**, 712–724 (2006).
18. P. R. K. Stephen Y.Chou and P. J. Renstrom, "Imprint lithography with 25-nanometer resolution," Science **272** (1996).
19. E. T. J. Batey, "Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition," J. Appl. Phys. **60**, 3136–3145 (1986).
20. L. L. Popovich, K. A. Gehoski, D. P. Mancini, and D. J. Resnick, "Bilayer and trilayer lift-off processing for i-line and DUV lithography," in *Optical Microlithography XV,* vol. 4691 (Proc. SPIE, 2002), pp. 899–906.
21. T. E. Wilson, K. A. Korolev, and N. A. Crow, "Bilayer lift-off process for aluminum metallization," J. Micro/Nanolithography, MEMS, MOEMS **14**, 014501:1–5 (2015).
22. S. Franssila and L. Sainiemi, *Reactive Ion Etching (RIE)* (Springer US, 2013), pp. 1–13.
23. A. Mahmoud and L. Wang, "A review of grazing incidence small- and wide-angle x-ray scattering techniques for exploring the film morphology of organic solar cells," Sol. RRL **5**, 2000337 (2020).
24. S. E. Fritz, S. M. Martin, C. D. Frisbie, M. D. Ward, and M. F. Toney, "Structural characterization of a pentacene monolayer on an amorphous sio2 substrate with grazing incidence x-ray diffraction," J. Am. Chem. Soc. **126**, 4084–4085 (2004).
25. M. C. Rowe and B. J. Brewer, "Amorph: A statistical program for characterizing amorphous materials by x-ray diffraction," Comput. & Geosci. **120**, 21–31 (2018).

26. L. Yang, Q. Cui, T. Liu, and C. Xue, "Effects of manufacturing errors on diffraction efficiency for multilayer diffractive optical elements," Appl. Opt. **50**, 6128–6133 (2011).
27. L. Zhao, Q. Cui, S. Mao, and Y. Hu, "Effect of the surface roughness on the efficiency of diffractive optical elements," Appl. Opt. **57**, 10276–10283 (2018).
28. Y. Shen, X. Wang, C. Min, X. Fu, Q. Liu, M. Gong, and X. Yuan, "Optical vortices 30 years on: Oam manipulation from topological charge to multiple singularities," Light. Sci. & Appl. **90** (2019).
29. H. Zhang, J. Zeng, X. Lu, Z. Wang, C. Zhao, and Y. Cai, "Review on fractional vortex beam," Nanophotonics **11**, 241–273 (2022).
30. J. N. Mait, G. W. Euliss, and R. A. Athale, "Computational imaging," Adv. Opt. Photon. **10**, 409–483 (2018).
31. G. Damberg, J. Gregson, and W. Heidrich, "High brightness hdr projection using dynamic freeform lensing," ACM Trans. Graph. **35**, 1–11 (2016).
32. F. Heide, M. Rouf, M. B. Hullin, B. Labitzke, W. Heidrich, and A. Kolb, "High-quality computational imaging through simple lenses," ACM Trans. Graph. **32**, 149:1–149:14 (2013).
33. M. Dimaki, M. Vergani, A. Heiskanen, D. Kwasny, L. Sasso, M. Carminati, J. A. Gerrard, J. Emneus, and W. E. Svendsen, "A compact microelectrode array chip with multiple measuring sites for electrochemical applications," Sensors **14**, 9505–9521 (2014).
34. P. K. Tyagi, E. Friebe, B. Jacques, T. Goulet, and S. Travers, "Reduction of spikes on the sides of patterned thin films for magnetic tunnel junction based molecular device fabrication," (2019).
35. C. H. Jeong, J. H. Lee, J. T. Lim, N. G. Cho, C. H. Moon, and G. Y. Yeom, "Deposition of sio2 by plasma enhanced chemical vapor deposition as the diffusion barrier to polymer substrates," Jpn. J. Appl. Phys. **44**, 1022 (2005).